MOTOROLA

MCM145101

256 X 4 BIT STATIC RAM

The MCM145101 family of CMOS RAMs offers ultra low power and fully static operation with a single 5 volt supply. The CMOS 1024-bit devices are organized in 256 words by 4 bits. Separate data inputs and data outputs permit maximum flexibility in bus-oriented systems. Data retention at a power supply as low as 2.0 volts over temperature readily allows design into applications using battery backup for nonvolatility. The MCM145101 is fully static and does not require clocking in standby mode.

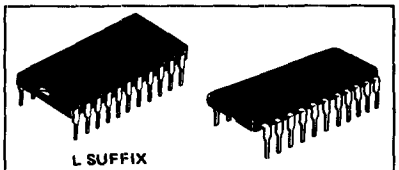
The MCM145101 is fabricated using the Motorola advanced ion-implanted, silicon-gate technology for high performance and high reliability.

- Low Standby Power
- Fast Access Time
- Single + 5.0 Volt Supply
- Fully TTL Compatible—All Inputs and Outputs
- Three-State Output
- Fully Static Operation
- Data Retention to 2.0 Volts
- Direct Replacement for:
  - Intel 5101 Series
  - AMI S5101 Series
  - Hitachi MH435101 Series
- Pin Replacement for Harris HM6501 Series

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

1024-BIT STATIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 736

P SUFFIX
PLASTIC PACKAGE
CASE 708

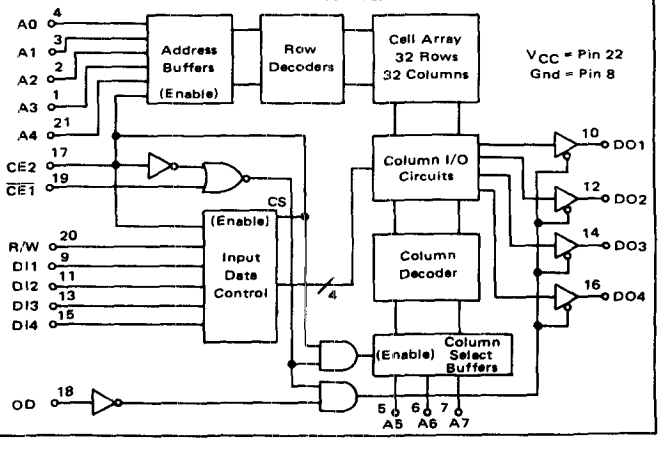
ORDERING INFORMATION

MCM14XXXX — Suffix Denotes
- L
- P
- -1
- -3
- -8
- (Not Used)

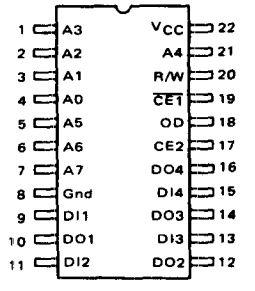
Selections for speed and power (see table)

Type Number	Typical Current @ 2 Vdc (μA)	Typical Current @ 5 Vdc (μA)	Max Access (ns)
MCM145101L, MCM145101P	0.14	0.2	650
MCM145101-1L, MCM145101-1P	0.14	0.2	450
MCM145101-3L, MCM145101-3P	0.70	1.0	650
MCM145101-8L, MCM145101-8P	–	10	800

BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

$\overline{CE1}$	CE2	OD	R/W	D_{In}	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D_{In}	Write
L	H	L	H	X	D_{Out}	Read

MAXIMUM RATINGS (Voltages referenced to V_{SS} Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Voltage on Any Pin	V_{in}	-0.3 to V_{CC} +0.3	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

DC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5 V ±5%)

Characteristic	Symbol	MCM145101,-1			MCM145101-3			MCM145101-8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Current	I_{in}(2)	–	5.0	–	–	5.0	–	–	5.0	–	nAdc
Input High Voltage	V_{IH}	2.2	–	V_{CC}	2.2	–	V_{CC}	2.2	–	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.65	-0.3	–	0.65	-0.3	–	0.65	Vdc
Output High Voltage (I_{OH} = -1.0 mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	Vdc
Output Leakage Current ($\overline{CE1}$ = 2.2 V, V_{OL} = 0 V to V_{CC})	I_{LO}(2)	–	–	±1.0	–	–	±1.0	–	–	±2.0	μAdc
Operating Current (V_{in} = V_{CC}, except $\overline{CE1}$ < 0.65 V, outputs open)	I_{CC1}	–	9.0	22	–	9.0	22	–	11	25	mAdc
Operating Current (V_{in} = 2.2 V, except $\overline{CE1}$ < 0.65 V, outputs open)	I_{CC2}	–	13	27	–	13	27	–	15	30	mAdc
Standby Current (CE2 < 0.2 V)	I_{CCL}(2),(4)	–	–	10	–	–	200	–	–	500	μAdc

CAPACITANCE

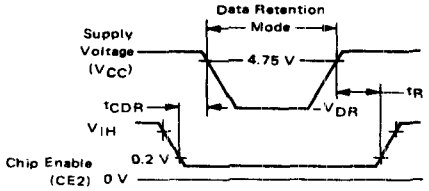
Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	8.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12.0	pF

LOW V_{CC} DATA RETENTION CHARACTERISTICS (Excluding MCM145101-8) T_A = 0°C to 70°C

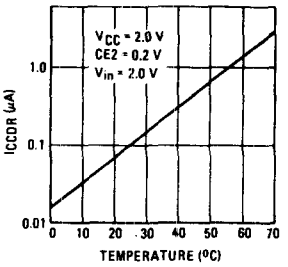
Parameter	Test Conditions		Symbol	Min	Typ.(1)	Max	Units
V_{CC} for Data Retention	CE2 < 0.2 V		V_{DR}	2.0	–	–	Vdc
MCM145101 or MCM145101-1 Data Retention Current		V_{DR} = 2.0 V,	I_{CCDR1}	–	0.14	10	μAdc
MCM145101-3 Data Retention Current		V_{DR} = 2.0 V,	I_{CCDR2}	–	0.70	200	μAdc
Chip Deselect to Data Retention Time			t_{CDR}	0	–	–	ns
Operation Recovery Time			t_R	t_{RC}(3)	–	–	ns

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage.
2. Current through all inputs and outputs included in I_{CCL} measurement.
3. t_{RC} = Read Cycle Time.
4. Low current state is for CE2 = 0 only.

LOW V_{CC} DATA RETENTION WAVEFORM



TYPICAL I_{CCDR} versus TEMPERATURE



AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	+0.65 V to 2.2 V
Input Rise and Fall Times	20 ns
Output Load —	1 TTL Gate and C_L = 100 pF
Timing Measurement Reference Level	1.5 Volt

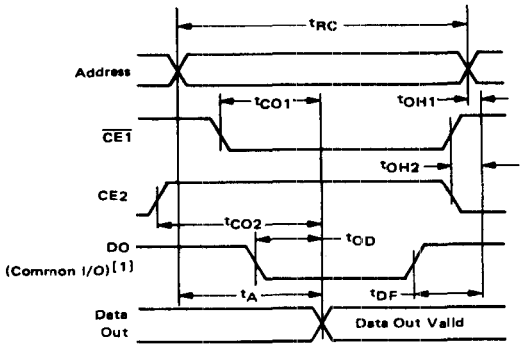
READ CYCLE

Parameter	Symbol	MCM145101-1		MCM145101,-3		MCM145101-8	
		Min	Max	Min	Max	Min	Max
Read Cycle	t_{RC}	450	–	650	–	800	–
Access Time	t_A	–	450	–	650	–	800
Chip Enable ($\overline{CE1}$) to Output	t_{CO1}	–	400	–	600	–	800
Chip Enable (CE2) to Output	t_{CO2}	–	500	–	700	–	850
Output Disable to Output	t_{OD}	–	250	–	350	–	450
Data Output to High Z State	t_{DF}	0	130	0	150	0	200
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0	–	0	–	0	0
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0	–	0	–	0	0

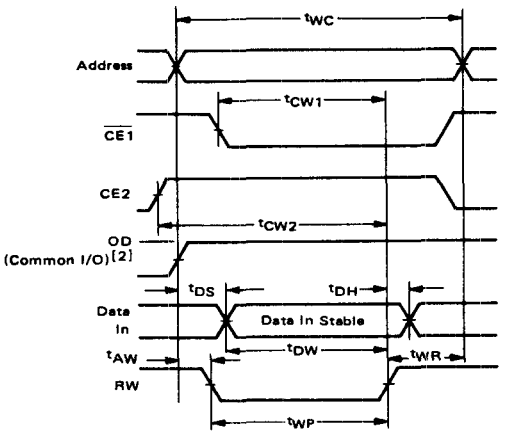
WRITE CYCLE

Write Cycle	t_{WC}	450	–	650	–	800	–
Write Delay	t_{AW}	130	–	150	–	200	–
Chip Enable ($\overline{CE1}$) to Write	t_{CW1}	350	–	550	–	650	–
Chip Enable (CE2) to Write	t_{CW2}	350	–	550	–	650	–
Data Setup	t_{DW}	250	–	400	–	450	–
Data Hold	t_{DH}	50	–	100	–	100	–
Write Pulse	t_{WP}	250	–	400	–	450	–
Write Recovery	t_{WR}	50	–	50	–	100	–
Output Disable Setup	t_{DS}	130	–	150	–	200	–

READ CYCLE TIMING

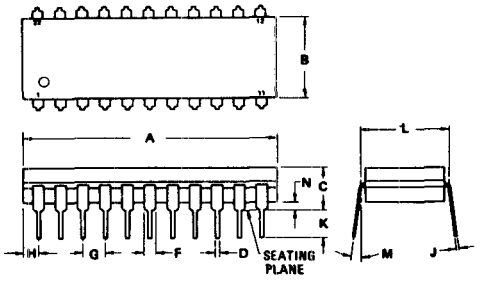


WRITE CYCLE TIMING



NOTES: 1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

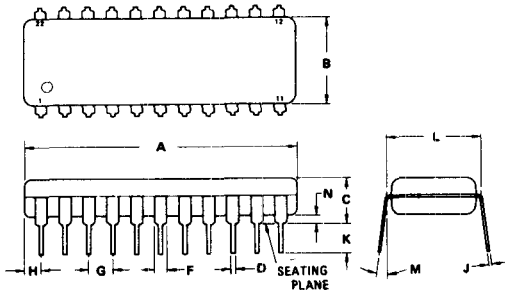
PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	26.80	27.81	1.055	1.095
B	9.14	9.91	0.360	0.390
C	3.81	5.46	0.150	0.215
D	0.38	0.53	0.015	0.021
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	2.54	4.32	0.100	0.170
L	9.91	10.41	0.390	0.410
M	–	15°	–	15°
N	0.25	0.89	0.010	0.035

CERAMIC PACKAGE
CASE 736-01

NOTES:
1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "D").
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	28.83	29.59	1.135	1.165
B	8.64	9.14	0.340	0.360
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	9.65	10.16	0.380	0.400
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

PLASTIC PACKAGE
CASE 708-01